SPT7883
10-bit, 70 MSPS A/D Converter

Features

- 2.5V power supply
- SNR: 59.5dB @ f_{IN} = 10MHz, f_S = 70 MSPS;
  57dB @ f_{IN} = 30MHz
- Low power dissipation: 129mW @ 2.5V;
  Sleep mode: 17mW
- Sample rate: 10–115 MSPS
- Frequency-dependent biasing
- Internal sample-and-hold
- Differential input
- Low input capacitance
- 9.5 ENOBs @ f_{IN} = 10MHz, f_S = 70 MSPS
- SFDR: 77.5dB

Applications

- Imaging
- Computer scanners
- Communications
- Set top boxes
- Video products
- Battery-operated equipment
- Portable test equipment

Description

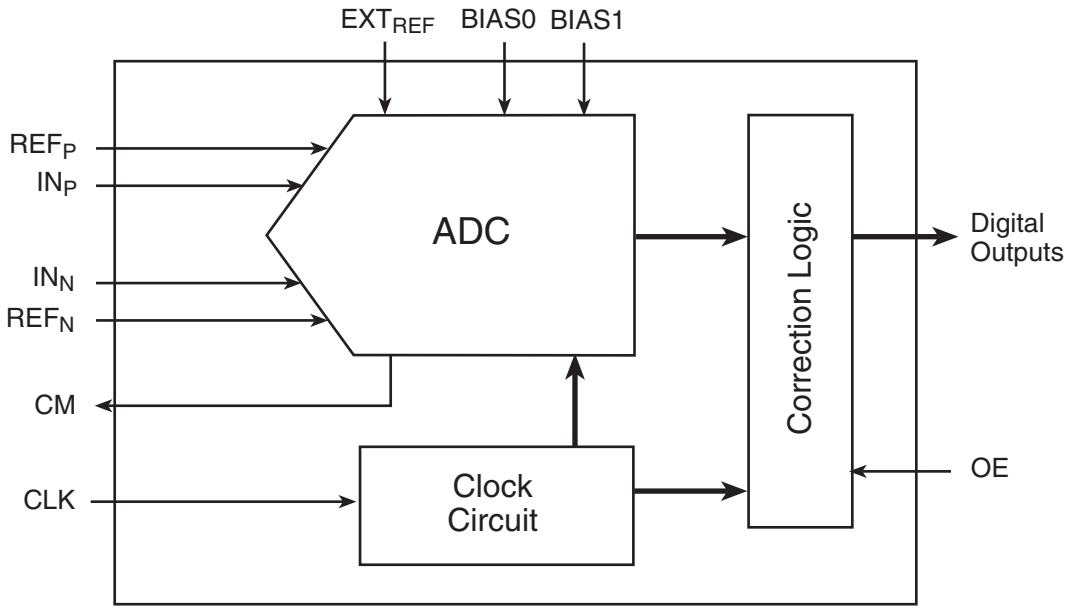
The SPT7883 is a compact, high-speed, low-power 10-bit monolithic analog-to-digital converter, implemented in a 0.25µm CMOS process. It has 10-bit resolution with 9.5 effective bits and spurious-free dynamic range (SFDR) of 77.5dB for 10MHz input signals. The converter includes a high bandwidth sample-and-hold. The full-scale range can be set between ±0.5V and ±1.5V. It operates from a single 2.5V supply. Its low distortion and high dynamic range provide the performance needed for demanding imaging, video, and communications applications.

The bias current level for the ADC is automatically adjusted based on the clock input frequency. Hence, the power dissipation of the device is continuously optimized for the operating frequency.

The SPT7883 has a pipelined architecture, resulting in low input capacitance. Digital error correction of the 9 most significant bits ensures good linearity for input frequencies approaching Nyquist.

The SPT7883 is available in a 28-lead SSOP package over the industrial temperature range (-40°C to +85°C).

Block Diagram



Absolute Maximum Ratings (beyond which damage may occur)[1] 25°C

Parameter	Min.	Max.	Unit
Supply Voltages			
V_{DD}	-0.3	+3	V
OV_{DD}	-0.3	V_{DD} +0.3	V
Input Voltages			
Digital Inputs	-0.3	V_{DD} +0.3	V
REF_P, REF_N	-0.3	V_{DD} +0.3	V
IN_P, IN_N	-0.3	V_{DD} +0.3	V
CLK	-0.3	V_{DD} +0.3	V
Temperature			
Operating Temperature	-40	+85	°C
Storage Temperature	-65	+150	°C
ESD Sensitivity on Input Pins 23 and 24			
Human Body Model	300		V
Machine Model	25		V

Note:

1. Operation at any absolute maximum rating is not implied.
   See Electrical Specifications table for proper nominal applied conditions in typical applications.

Electrical Specifications

(T_A = 25°C, V_{DD} = OV_{DD} = 2.5V, f_S = 70 MSPS, f_{IN} = 10MHz, internal references, differential input signal, 50% duty cycle, typical bias; unless otherwise noted)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Unit
DC Performance	f_{IN} = 1kHz					
Differential Linearity Error (DLE)		V		±0.35		LSB
Integral Linearity Error (ILE)		V		±0.55		LSB
No Missing Codes		IV		Guaranteed		
Offset Error (V_{os})		V		±4.8		mV
Gain Error		V		±1.5		%FS
Dynamic Performance						
Signal-to-Noise & Distortion (SINAD)	f_{IN} = 10MHz	I	56.2	59		dBc
	f_{IN} = 30MHz	V		56.5		dBc
Signal-to-Noise Ratio (SNR)	f_{IN} = 10MHz	I	56.9	59.5		dBc
	f_{IN} = 30MHz	V		57		dBc
Total Harmonic Distortion (THD)	f_{IN} = 10MHz	I	-61.0	-72.5		dBc
	f_{IN} = 30MHz	V		-66		dBc
Spurious Free Dynamic Range (SFDR)	f_{IN} = 10MHz	V		77.5		dBc
	f_{IN} = 30MHz	V		71		dBc
Effective Number of Bits (ENOB)	f_{IN} = 10MHz	I	9.0	9.5		Bits
	f_{IN} = 30MHz	V		9.1		Bits
Analog Input						
Input Voltage Range (differential)		IV	±0.5	±1.0	±1.5	V
CMRR (V_{os})	0.75V to 1.75V	V		60		dB
Analog Input Bandwidth		V		133		MHz

NOTE: All electrical characteristics are subject to the following condition:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Electrical Specifications

(T_A = 25°C, V_{DD} = OV_{DD} = 2.5V, f_S = 70 MSPS, f_{IN} = 10MHz, internal references, differential input signal, 50% duty cycle, typical bias; unless otherwise noted)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Unit
Timing Characteristics						
Max Conversion Rate	See graph pg 4	IV	70			MHz
Min Conversion Rate		IV			10	MHz
Pipeline Delay	See Timing Diag. pg 6	V		6		Cycles
Power Supply Requirements						
Supply Voltage (V_{DD})		IV	2.3	2.5	2.75	V
Output Driver Supply Voltage (OV_{DD})		IV	1.75	2.5	2.75	V
Supply Current (I_{VDD} + I_{OVDD})	f_S = 70 MSPS; f_{IN} = 10MHz	I		52	64	mA
PSRR (V_{os})	2.25V to 2.75V	V		60		dB
Power Dissipation	f_S = 70 MSPS; f_{IN} = 10MHz	I		129	160	mW
Sleep Mode Power Dissipation	f_S = 70 MSPS; f_{IN} = 10MHz	V		17		mW
Reference Voltages						
Internal Ref Voltage Pos (V_{REFP})	EXT_{REF} = 0	I	1.67	1.75	1.83	V
Internal Ref Voltage Neg (V_{REFN})	EXT_{REF} = 0	I	0.67	0.75	0.83	V
Common Mode Output Voltage (V_{CM})		I	1.17	1.25	1.33	V
Reference Temperature Coefficient		V		250		ppm/°C
External Positive Input Voltage	EXT_{REF} = 1	IV	1.5	1.75	2.0	V
External Negative Input Voltage	EXT_{REF} = 1	IV	0.5	0.75	1.0	V
Reference Input Voltage Range		IV	0.5		2.0	V
Digital Inputs						
Logic “0” Voltage		I			0.5	V
Logic “1” Voltage		I	2.0			V
Logic “0” Current (V_I = V_{GND})		I			±10	µA
Logic “1” Current (V_I = V_{DD})		I			±10	µA
Digital Outputs						
Logic “1” Voltage	I = -2mA	I	85% OV_{DD}	90% OV_{DD}		V
Logic “0” Voltage	I = 2mA	I		0.2	0.4	V
Timing Characteristics						
CLK Fall to Output Data Valid (t_D)	C_{LOAD} = 25 pF	IV		7.5	8.5	ns
Rise Time (t_R)	C_{LOAD} = 25 pF	V		3.5		ns
Fall Time (t_F)	C_{LOAD} = 25 pF	V		3.5		ns

NOTE: All electrical characteristics are subject to the following condition:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and quality assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

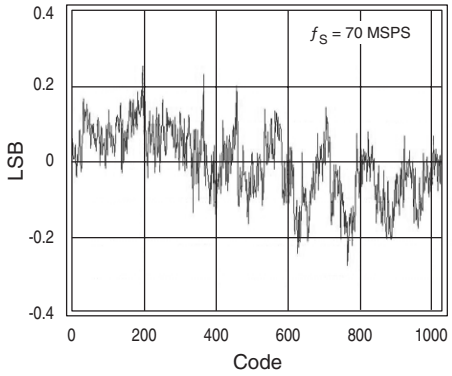
TEST LEVEL CODES:

Level	Test Procedure
I	100% production tested at the specified temperature.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

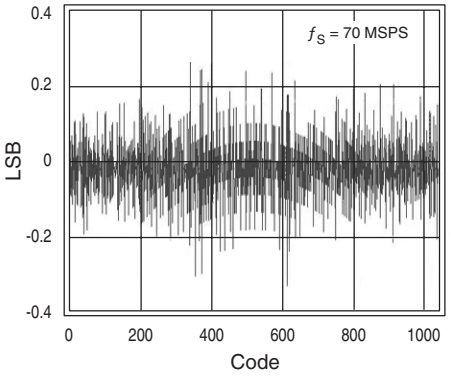
Typical Operating Characteristics

(T_A = 25°C, V_{DD} = OV_{DD} = 2.5V, internal references, differential input signal, 50% duty cycle, typical bias; unless otherwise noted)

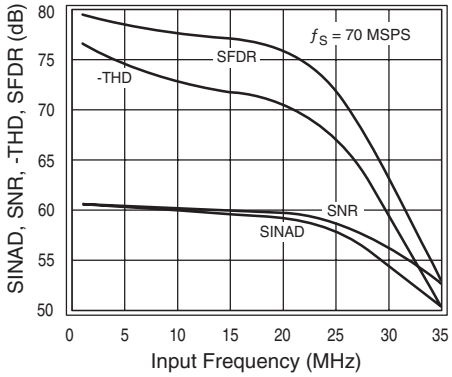
ILE vs. Code



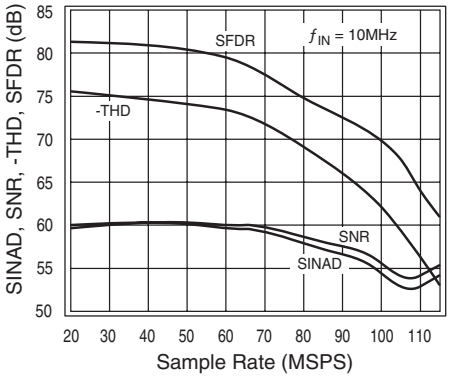
DLE vs. Code



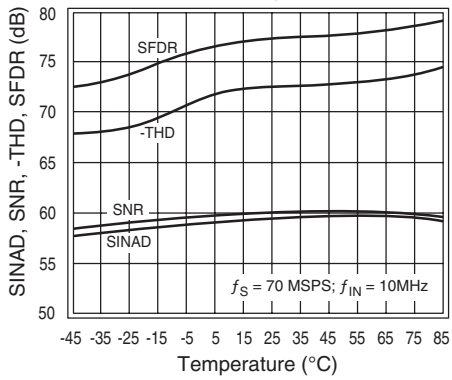
Performance vs. Input Frequency



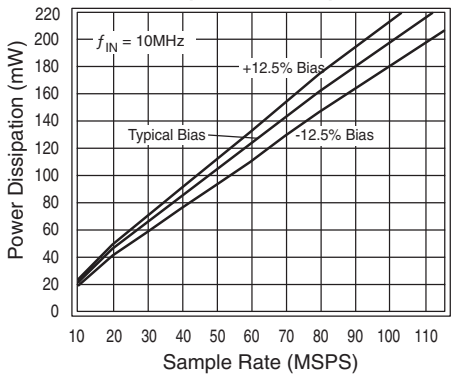
Performance vs. Sample Rate



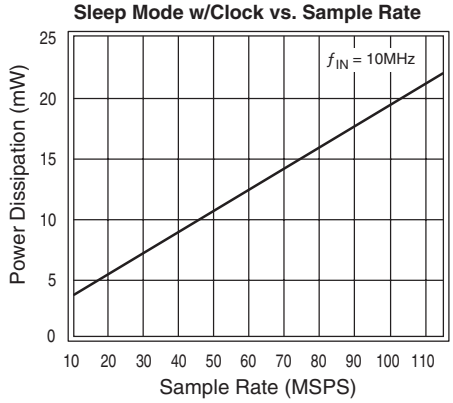
Performance vs. Temperature



Power Dissipation vs. Sample Rate



Sleep Mode w/Clock vs. Sample Rate



References

The SPT7883 can use either an internal or external voltage reference. When the digital input EXT_{REF} is high, the external reference is used. When EXT_{REF} is low, the internal reference is used.

Internal Reference

The internal references are set at +0.75V and +1.75V. When the internal reference is used, the full-scale range of the analog input is set at ±1.0V differential. Do not connect external references when the internal reference is used. Internal references are valid when the clock signal is present.

External Reference

When external references are used, the voltages applied to the V_{REF_P} and V_{REF_N} pins determine the input voltage range, which is equal to ± (V_{REF_P} – V_{REF_N}). Externally generated reference voltages must be connected to these pins and should be symmetric about the common mode voltage (1.25V).

Analog Input

The SPT7883 has a differential input that should have a common mode voltage of 1.25V. The input voltage range is determined by the reference voltages, which may be generated internally or applied externally.

The input of the SPT7883 can be configured in various ways depending on whether a single-ended or differential, AC- or DC-coupled input is desired.

AC-coupled input is most conveniently implemented using a transformer with a center-tapped secondary winding. The center tap is connected to the CM node, as shown in Figure 1. In order to obtain low distortion, it is important that the selected transformer does not exhibit core saturation at full scale. Excellent results are obtained with the Mini-Circuits T1-6T or T4-6T. Proper termination of the input is important for input signal purity. A 50Ω resistor in series with each input and a small capacitor (typ 27pF) across the inputs will attenuate kickback noise from the sample-and-hold.

If a DC-coupled single-ended input is wanted, a solution based on operational amplifiers is usually preferred. The AD8138 is an easy-to-use, single-ended-to-differential converter. Its data sheet claims –87 dBc @ 20MHz. Lower-cost operational amplifiers may be used if the demands are less strict.

The analog inputs (pins 23 and 24) are sensitive to ESD, and proper precautions are required.

Clock

In order to preserve accuracy at high input frequency, it is important that the clock have low jitter and fast rise and fall times. Rise/fall times should be less than 2ns whenever possible. Overshoot should be minimized. Low jitter is especially important when converting high-frequency input signals. Jitter causes the noise floor to rise proportionally to input signal frequency. The analog input is sampled at the falling edge of the clock.

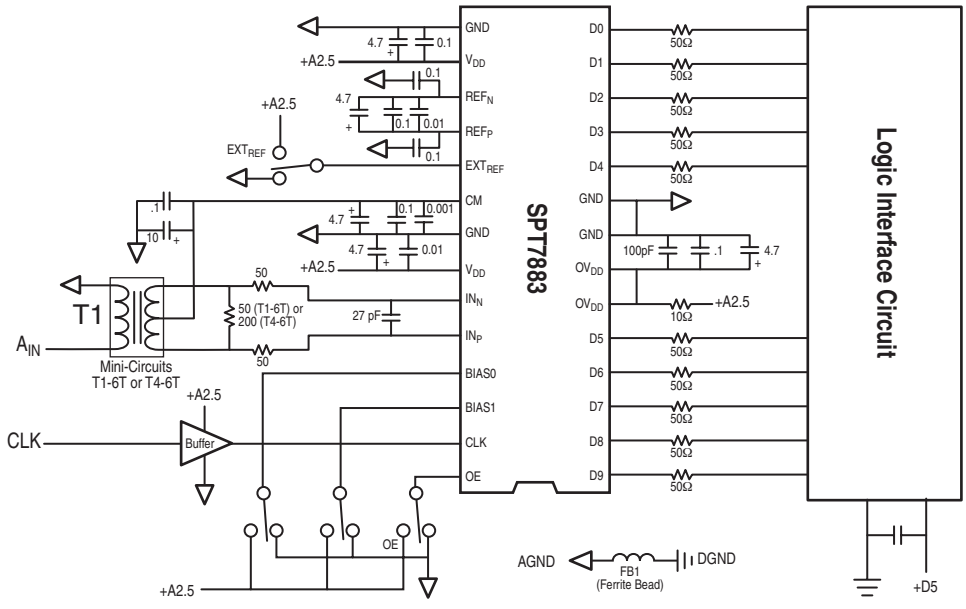


Figure 1. Typical Interface Circuit Diagram

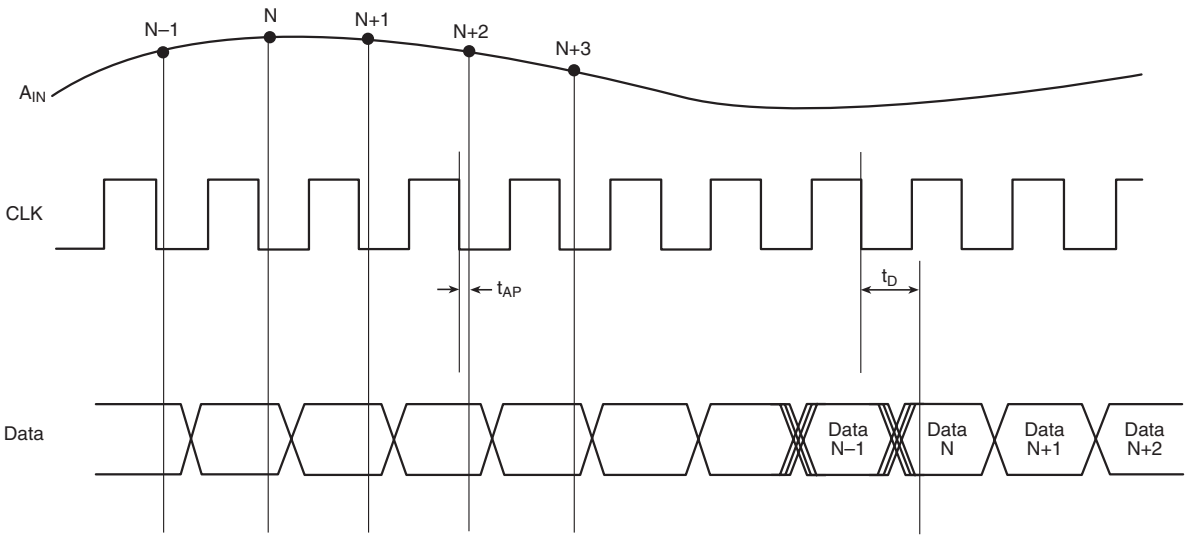


Figure 2. Timing Diagram

Digital Outputs

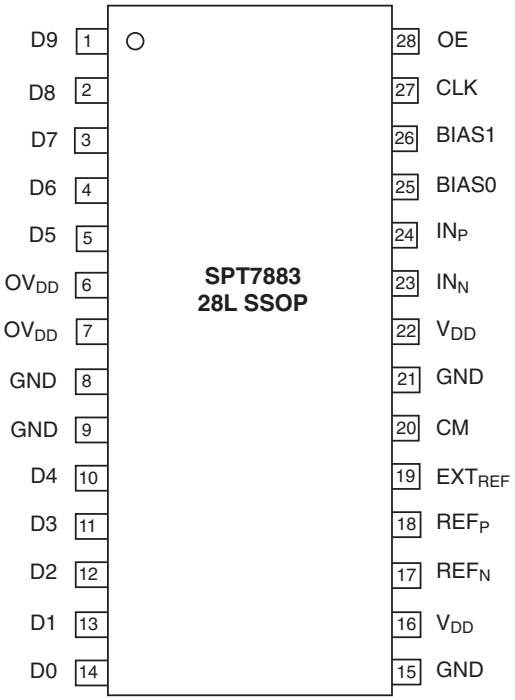
When the output enable is set high, then the digital output data appears in offset binary code at CMOS 2.5V logic levels. Full-scale negative input results in output code 000…0. Full-scale positive input results in output code 111…1. Output data is available 6 clock cycles after the data is sampled. The analog input is sampled one aperture delay (t_{AP}) after the high-to-low clock transition. Output data should be sampled as shown in the timing diagram above.

When the output enable is set low, then the digital output data goes into a high-Z mode.

PCB Layout and Decoupling

A well designed PCB is necessary to get good spectral purity from any high-performance ADC. A multilayer PCB with a solid ground plane is recommended for optimum performance. If the system has a split analog and digital ground plane, it is recommended that all ground pins on the ADC be connected to the analog ground plane (AGND). All digital interface circuits are connected to the digital ground (DGND). AGND and DGND planes must be connected through a ferrite bead placed as close to the ADC as possible. Refer to the *Typical Interface Circuit Diagram* (Figure 1) or AN7883 application note for recommended decoupling and PCB layout.

Pin Assignments



Pin Definitions

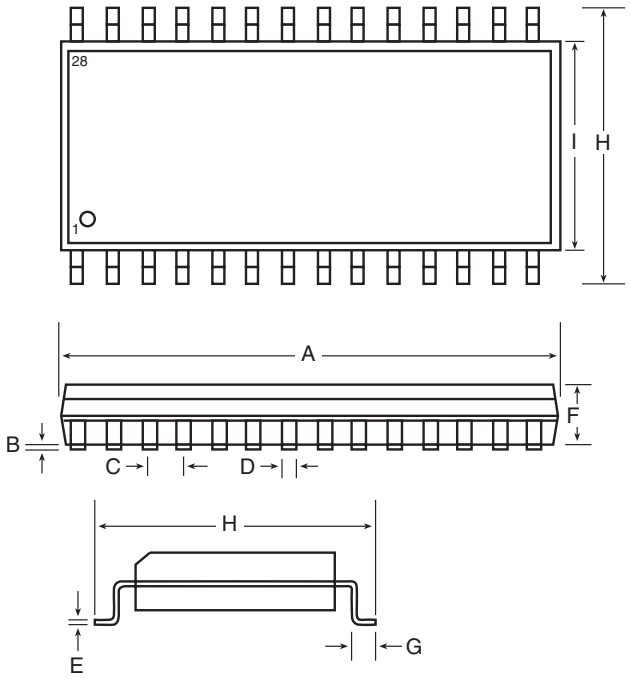
Pin Name	Description
IN_P IN_N	Differential input signal pins. Common-mode voltage: 1.25V
REF_P REF_N	Reference I/O pins.
BIAS0, BIAS1	BIAS1 = 0, BIAS0 = 0: Sleep mode (power save)
	BIAS1 = 0, BIAS0 = 1: -12.5% bias
	BIAS1 = 1, BIAS0 = 0: +12.5% bias
	BIAS1 = 1, BIAS0 = 1: typ bias
CLK	Clock input
CM	Common mode voltage output
D9–D0	Digital outputs (MSB to LSB)
OE	Enable digital outputs
	Logic 1: digital output enable
	Logic 0: tri-state
EXT_{REF}	Digital input: reference select
	EXT_{REF} = 1: use external reference. Internal reference powered down.
	EXT_{REF} = 0: internal reference is used.
V_{DD}	Power supply pins
GND	Ground pins
OV_{DD}	Power supply pins for output drivers

Ordering Information

Model	Part Number	Package
SPT7883	SPT7883SIR	SSOP-28

Temperature range for all parts: -40°C to +85°C.

Package Dimensions



SSOP-28						
	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A	0.397		0.407	10.07		10.33
B	0.002		0.008	0.05		0.21
C		0.0256			0.65	
D	0.010		0.015	0.25		0.38
E	0.004		0.008	0.09		0.20
F	0.066		0.070	1.68		1.78
G	0.025		0.037	0.63		0.95
H	0.301		0.311	7.65		7.90
I	0.205		0.212	5.20		5.38